

Atty. Docket No. PIA31075/DBE/US
Serial No: 10/750,246

Amendments to the Claims

Please add new claims 10-19, and amend claims 5 and 8 as follows:

1. (Previously Presented) A method of removing polymer generated in a semiconductor manufacturing process, which includes sequentially depositing a lower metal layer, an insulating layer and an upper metal layer on a semiconductor substrate; forming a photoresist pattern on the upper metal layer; and etching the upper metal layer and the insulating layer by using the photoresist pattern as a mask, the polymer being generated during the etching step, the method comprising:

- (a) removing the photoresist pattern by using O_2/N_2 plasma; and
- (b) removing the polymer existing on the lower metal layer by using H_2O/CF_4

plasma.

2. (Original) A method as defined by claim 1, wherein (a) is carried out for about 50 seconds.

3. (Original) A method as defined by claim 1, wherein a flow rate of a CF_4 gas in (b) is in a range from 5% to 15% of that of an H_2O gas.

4. (Original) A method as defined by claim 1, further comprising (c) by using O_2 plasma, removing residues of the photoresist pattern remaining after (b).

5. (Currently Amended) A ~~methods~~ method as defined by claim 4, wherein ~~powered powers used~~ in the (a), (b) and (c) are substantially the same.

6. (Original) A method as defined by claim 4, wherein a process time of (c) is in a range from 40% to 60% of that of (a).

Atty. Docket No. PLA31075/DBE/US
Serial No: 10/750,246

7. (Original) A method as defined by claim 4, wherein a process time of (b) is in a range of 30% to 50% of that of (a).

8. (Currently Amended) A method of manufacturing a semiconductor device having a capacitor, the method comprising:

(a) sequentially depositing a lower metal layer, an insulating layer and an upper metal layer on a semiconductor substrate;

(b) forming a first photoresist pattern on the upper metal layer;

(c) forming an upper electrode film and a capacitor insulating film by etching the upper metal layer and the insulating layer by using the first photoresist pattern as a mask;

(d) removing the first photoresist pattern by using O_2/N_2 plasma;

(e) removing polymer existing on the lower metal layer by using H_2O/CF_4 plasma;

(f) forming a second photoresist pattern for completely encapsulating the upper electrode film and the capacitor ~~insulating~~ insulating film;

(g) forming a lower electrode film by etching the lower metal layer by using the second photoresist pattern as a mask and

(h) removing the second photoresist pattern to provide the capacitor including the lower electrode film, the capacitor insulating film and the upper electrode film.

9. (Original) A method as defined by claim 8, further comprising, between (e) and (f): removing residues of the first photoresist pattern remaining after (e) by using O_2 plasma.

10. (New) A method of removing polymer from a lower metal layer having an insulating layer and an upper metal layer thereon, the lower metal layer on a semiconductor substrate, the upper metal layer having a first photoresist pattern thereon, the method comprising steps of:

Atty. Docket No. PIA31075/DBE/US
Serial No: 10/750,246

(a) removing the first photoresist pattern by ashing with a first plasma from a first gas mixture consisting essentially of O_2 and N_2 ; and

(b) removing the polymer on the lower metal layer by ashing with a second plasma from a second gas mixture consisting essentially of H_2O and CF_4 .

11. (New) A method as defined by claim 10, wherein step (a) is carried out for about 50 seconds.

12. (New) A method as defined by claim 10, wherein step (b) comprises flowing CF_4 gas at a rate of from 5% to 15% of that of H_2O gas.

13. (New) A method as defined by claim 10, further comprising:

(c) removing residues of the first photoresist pattern remaining after step (b) with an O_2 plasma.

14. (New) A method as defined by claim 13, wherein steps (a), (b) and (c) each use substantially the same power.

15. (New) A method as defined by claim 13, wherein a process time of step (c) is from 40% to 60% of that of step (a).

16. (New) A method as defined by claim 10, wherein a process time of step (b) is from 30% to 50% of that of step (a).

17. (New) The method of claim 10, further comprising, prior to step (a), steps of sequentially depositing the lower metal layer, the insulating layer and the upper metal layer on the semiconductor substrate; forming the first photoresist pattern on the upper metal layer; and

Atty. Docket No. PIA31075/DBE/US
Serial No: 10/750,246

forming an upper electrode by etching the upper metal layer using the first photoresist pattern as a mask.

18. (New) The method of claim 17, further comprising, after forming the upper electrode and prior to step (a), forming a capacitor insulating film by etching the insulating layer using the first photoresist pattern as a mask.

19. (New) The method of claim 18, further comprising, after step (b), steps of forming a second photoresist pattern completely encapsulating the upper electrode and the capacitor insulating film; forming a lower electrode by etching the lower metal layer using the second photoresist pattern as a mask; and removing the second photoresist pattern to provide a capacitor including the lower electrode film, the capacitor insulating film and the upper electrode film.